A Time-of-Flight 3-D Image Sensor With Concentric-Photogates Demodulation Pixels

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***Abstract*— In this paper, we develop pixels with concentric-photogates for applications in time-of-flight 3-D image sensors with single-tap architecture. The pixel uses a buried-channel device and features a reduced effective electron transit length, for the rapid transfer of a signal electron. A reduction in the interpixel irregularity of signal levels and a consequent increase in the demodulation signal amplitude are observed in the single-tap operation mode as opposed to the multitap operation mode. Specifically, we are able to achieve a demodulation contrast higher than 50% from 20 MHz modulation of an 850 nm light-emitting diode illumination. Finally, we construct a sensor composed of 198 × 108 concentric photogate pixels, each with a pitch of 28 μm, and use it to generate a 3-D image conveying gross distance information and detailed object features with a distance error of less than 1% over a range of 1 to 7 m.**

***Index Terms*— 3-D, CMOS, image sensor, phase-shift demodulation, photogate, time-of-flight (ToF).**

I. Introduction

ADVANCES made in the CMOS image sensor (CIS) industry have led to the development of simple operation principles, cost-effective fabrication technologies, and miniaturization-friendly architectures. Such advancements, along with simpler optic modules, have allowed for time-of-flight (ToF) 3-D image sensors to emerge as a viable alternative to stereo and structured light imaging for capturing range information [1]. Yet, further improvements in the performance of 3-D imaging are critical for mass adoption by the consumer electronics industry for applications such as gesture-control user interfaces, safety applications, and the generation of 3-D contents.

A ToF-3-D camera is typically composed of a modulating light source such as a light-emitting diode (LED) or a laser diode (LD) of near-infrared (NIR) wavelength, and a demodulating pixel array [2], as schematically shown in Fig. 1. An array of LEDs and image sensor are located on approximately the same optical plane. Reflection of the modulated LED light from an object located at a distance R from the camera brings about a phase-shift, φ. Accordingly R can be obtained from the principle of ToF as detailed in the following equation:

$$R = \frac{c}{4\pi f} \cdot \varphi \tag{1}$$

where c is the speed of light and f is the modulation frequency. The choice of modulation frequency used in ToF measurements depends on the distance between the light source and object; for operational range R up to 7.5 m, the appropriate f is 20 MHz. The pixel array is capable of capturing phase-sensitive images with respect to the LED modulation of period $p = 1/f$; images with controlled phases of $p \cdot k/4$ with $k = 0, 1, 2$, and 3, are captured in synchronization with the LED modulation. Assuming a sinusoidally modulated LED illumination, φ for such phase-sensitive images with corresponding signal level S_k can be evaluated using the following equation:

$$\varphi = \tan^{-1}\left(\frac{S_3 - S_1}{S_0 - S_2}\right). \tag{2}$$

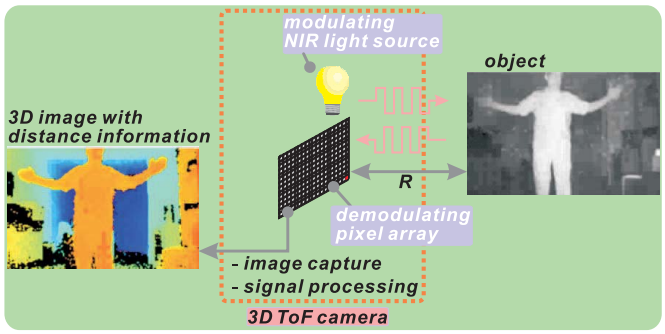

Fig. 1. Scheme detailing the ToF-3-D image acquisition of an object located at distance R from a camera. A modulating NIR light source such as an 850 nm wavelength LED is irradiated on the object. The reflected light incident on the camera conveys phase-shift, which is extracted from the demodulation pixel array. At high speeds, such as 20 MHz, synchronized control of modulation and demodulation of the LED and pixel is required to reduce DE. With proper image signal processing, which includes pixel-wise calculations of phase-shift using (1) to (2), a 3-D image containing range information is produced.

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Subsequent signal processing, including pixel-wise calculations using (1) and (2), yields a 3-D image conveying range information.

A key performance metric of 3-D imaging is the precision of range information. Once the uncertainty of measured distance R is represented by its standard deviation σ_R, the precision of range information is represented as distance error (DE), conventionally defined as a ratio of σ_R to R, or the following:

$$\mathrm{DE} = \frac{\sigma_R}{R}. \tag{3}$$

Compiling (1) to (3), DE can be expressed in the following manner [2]:

$$\mathrm{DE} = \frac{1}{\sqrt{2}} \cdot \frac{1}{\mathrm{DC} \cdot \sqrt{B}} \cdot \sqrt{1 + \frac{N}{B}} \tag{4}$$

where N is the contribution from dark and temporal noises and DC is the demodulation contrast defined as

$$\mathrm{DC} = \frac{A}{B} = 2 \cdot \frac{\sqrt{(S_0 - S_2)^2 + (S_1 - S_3)^2}}{S_0 + S_1 + S_2 + S_3} \tag{5}$$

where A and B correspond to the amplitude and offset of the demodulated signal, respectively, and are defined as follows:

$$A = \frac{\sqrt{(S_0 - S_2)^2 + (S_1 - S_3)^2}}{2} \tag{6}$$

$$B = \frac{S_0 + S_1 + S_2 + S_3}{4}. \tag{7}$$

It should be noted that B is critically determined by the quantum efficiency (QE) of the pixel, and independent of phase-shift due to the periodicity of the modulating light. Furthermore, N/B corresponds to the ratio of dark and temporal noise-level to signal level.

As evident from from (4), a reduction in DE can be achieved via an enhancement in DC, QE, signal-to-noise ratio (SNR), or a depression in the dark level. Various research efforts have been made to meet such goals, especially in pixel design [2]–[11]. Even though large pixels are helpful in improving SNR, a large drawback is the increase in dark level and degradation of the image spatial resolution. On the other hand, because the absorbance of Si is extremely low for NIR wavelengths, there are only a few methods to improve QE, such as optimized antireflection coating, use of a thick p-epi layer, fabrication with back-side-illumination architecture, and use of proper doping conditions for the pixel. In essence, improvements made to the DC can be considered the most effective method to reduce DE.

The most efficacious method to improve the DC is to enhance the charge transfer efficiency from the photon detecting section to the floating diffusion (FD) [7], [10]. In this paper, we propose a concentric photogate (CG) pixel for the reduction of effective carrier transit length, which induces a lateral electric field during photo-electron transport, while a relatively large pixel pitch of 28 μm is used to obtain acceptable SNR performance.

Additionally, the demodulation operation is executed via a "single tap" operation, viz. the sequential acquisition of S_k using a single signal output through a single FD, followed by calculations for distance using (1) and (2). To generate a single 3-D image, most ToF-3-D sensors capture in- and out-of-phase images from two independent FDs, relative to the modulated light (S_0 and S_2) during the first "field" of integration. In the following second integration field, the quadrature signals (S_1 and S_3) are captured, and complete the so-called two-tap operation. While the two-tap operation allows for an increase in signal capture rate, the pixel pair for two-tap operation requires careful matching among the independent signal outputs; in-phase and out-of-phase pixel nodes should be carefully designed to reproduce exactly the same charge transfer process and pixel conversion gain, as interpixel nonuniformity often results in the degradation of 3-D imaging performance. However, maintaining such symmetry is difficult to achieve, particularly as the pixel size is scaled down. The single-tap operation with single-tap pixels, as proposed in this paper, utilizes four fields of integration to collect four phase-sensitive images, thereby eliminating signal output matching requirements and ultimately reducing photoresponse nonuniformity (PRNU).

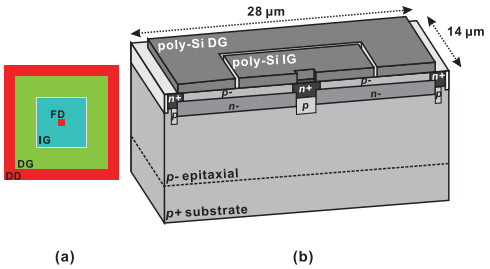

Fig. 2. (a) Schematic layout of a concentric-gate pixel composed of FD and DD, which surround an IG and a DG. (b) Cut-away view of a pixel showing a buried-channel structure. Photogates IG and DG are formed using poly-Si, while the gate dielectric—not shown in the diagram—is formed using thermally grown silicon oxide.

II. Concentric Photogate Pixel Architecture

The proposed concentric photogate pixel consists of a p-photodetecting epilayer on a p^+ substrate as shown in Fig. 2. In the center is an FD, which integrates the signal electrons, surrounded by two concentric gates. The inner gate (IG) is separated from the surrounding concentric outer drain gate (DG), which in turn is surrounded by a drain diffusion (DD). The latter can be in common with adjacent pixels.

Compared with conventional multitap pixels [2]–[5], [9], [11], the most distinctive features of the CG pixel can be found in its architecture facilitating rapid signal electron transport. Specifically, the transit length of signal electrons in a CG pixel is reduced to a radially directed half-pixel pitch due to the electric field under the IG and DG; the transit length is a full pixel pitch in a linear implementation of FD (e.g., in two-tap geometry). In addition, fine tuning of the doping profile can be implemented without concern for symmetry matching, an issue usually found among multitap structures. For example, a steep difference of electric potential between IG and DG coupled with the use of a proper doping profile under opposite bias conditions of IG and DG can enhance charge transfer around FD and DD, and simultaneously provide a clear signal charge separation between the two nodes.

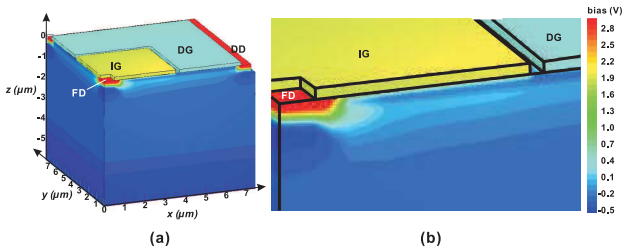

Fig. 3. Electric potential simulation of the quarterly vertical portion of a pixel after application of a 1.6 and 0.0 V bias to IG and DG, respectively, for 10 ns. (a) 3-D TCAD simulation results are used to construct a potential diagram zoomed-out near the FD region. (b) Closeup of the FD region indicates the formation of a buried channel with a lateral electrical field.

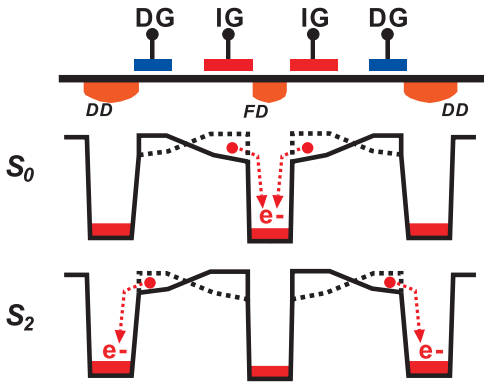

Fig. 4. Schematic illustrating the electron transfer process of a concentric-gate pixel during S_0 and S_2 integrations. During S_0 integration, a rapid transfer of charge to FD is anticipated because of the presence of a lateral electric field, while the transfer of charge to DD is prevented by a potential barrier. During S_2 integration, however, the bias to IG and DG is toggled to revert the potential around both FD and DD regions, thereby enabling the rapid transfer of charge to DD, and the inhibitions of transfer to FD. In this way, an increased demodulation contrast can be achieved during high-speed modulation of the IG and DG.

Furthermore, buried-channel devices are formed for the IG and DG, through which an increase in electron mobility is expected via a reduction in interface scattering. Finally, the generation of a fringing electric field—conventionally used in buried-channel charge-coupled devices as well as the previously reported ToF pixel [7], [10], [11]—promotes electron drift. A 3-D technology computer aided design (TCAD) simulation of electric potential, with a p^- layer of 1.0×10^{12} arbitrary unit (a.u.) dose and an n^- layer of 1.0×10^{11} a.u. dose, indicates a fairly uniform distribution of photoelectrons throughout the photoactive layer when illuminated with 850 nm NIR light (Fig. 3). Although most of the photo-electrons generated in the p^+ substrate are removed through recombination, those generated in the photoactive layer are collected and transferred primarily by drift; the carriers drift vertically toward the surface into the buried n-channel under the device, and are subsequently steered to either the FD or DD, depending on the biasing of the IG and DG.

The electron transfer process in the n-channel during in-phase and out-of-phase signal integration (S_0 and S_2) is outlined in a schematic potential diagram as in Fig. 4. During S_0 integration, the electric potential level of the DG is higher than that of the IG, and acts as a barrier for electron

TABLE I
NORMALIZED DOSE LEVELS USED IN p^- AND n^- LAYERS FORMATION

condition #	p^- layer with Boron (B)	n^- layer with Arsenic (As)
1	none	none
2	1.0	none
3	0.25	0.4
4	1.0	1.0

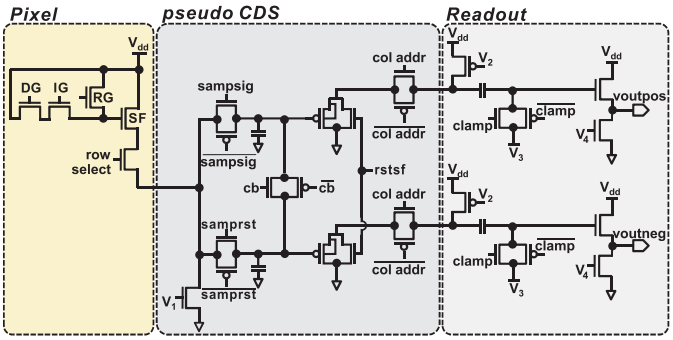

Fig. 5. Schematic diagram detailing the signal processing chain used to obtain field images from the test chip. Operation bias is set to V_{dd}, and the bias for pixel reset is also tied to V_{dd}. See text for a detailed description.

transfer to DD. Consequently, the potential gradient between the DG and IG steers lateral electron transfer toward the FD. The integration procedure of S_2 electrons occurs in an opposite manner, resulting in rapid electron transfer to DD and the prevention of transfer to FD. Thus, even at high frequency modulation of electronic potential, high-contrast and phase-sensitive charge collection becomes available, ultimately resulting in an enhanced DC.

It should be noted that at first glance, our pixel layout is similar to that of a previous report [12]. A closer look at the previous device, however, exhibits a two-tap architecture with a single photogate, and ring-gates surrounding FDs with a 100 μm pitch; the device architecture described in [12] is more similar to that described [4] or [9]. The working principle and pixel structure of our CG pixel is entirely different in that independent implementation of the IG and DG for each pixel suppresses interpixel cross talk, while the photogate is shared by all pixels in the device reported in [12].

III. FABRICATION AND EXPERIMENTAL

A 0.13 μm CMOS frontside-illuminated image sensor process was used in the fabrication of test chips with various p^- and n^- doping profiles as shown in Fig. 2. Dose levels for the formation of each p^- and n^- layer used in this paper are summarized in Table I; the maximum dose of p^- and n^- layers reaches approximately 1.0×10^{12} and 1.0×10^{11} a.u., respectively. In this paper, each pixel is fabricated with a p-epilayer of 3.0 μm thickness. The photogates of IG and DG devices were formed with polysilicon over a 67 Å thick thermal oxide layer on the photodetector area.

We used the signal chain schematically shown in Fig. 5, which has been employed in active pixel sensors with correlated-double-sampling (CDS) and readout circuitry [13]. The concentric-gate pixel is comprised of modulation gates IG

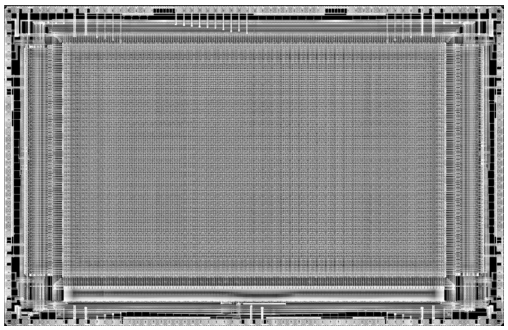

Fig. 6. Layout of a ToF-3-D image sensor chip, which consists of an array of 198 × 108 concentric-gate pixels, row-/column- drivers, and a circuit for pseudo-CDS.

and DG, drain node DD, reset gate RG, pixel source-follower SF, and "row select." To sense the photo-electron induced voltage drop from the reset level in FD, two nodes—"sampsig" and "samprst"—are used independently. The structure does not allow for normal CDS operation; the reset level is obtained after sampling of the signal level, and thus indicated as pseudo-CDS. Through proper operation of the nodes "cb" and "clamp," pseudo-CDS from "sampsig" and "samprst" is executed. With an appropriate application of biases to V_1, V_2, V_3, V_4, and enabling reset of column source followers with "rstsf," the analog signal is differentially read at "voutpos" and "voutneg" as V_{pos} and V_{neg}, respectively. Finally, the signal output is obtained as $\triangle V = V_{\text{pos}} - V_{\text{neg}}$.

The test chip is composed of an array of 192 × 108 pixels, row and column drivers, and circuitry for CDS and readout, as shown in Fig. 6. The reported sensor uses a fully flexible open architecture to enable off-chip implementation of timing control and analog-to-digital convertor (ADC).

Characterization of the test chip is performed with the timing schematically shown in Fig. 7. After reset, the selected first row with addresses "0," LED, IG, and DG begin to modulate. The (de)modulation period p is set to 50 ns with 50% duty ratio, corresponding to a 20 MHz (de)modulation frequency. Both the IG and DG toggle out of phase from each other. Phase-sensitivity of the obtained image is determined by the phase difference between LED and IG. Figure 7 exemplifies a case study using $p/4$ phase difference, corresponding to the acquisition of S_1 signal. Tuning the phase differences to 0, $p/2$, and $3p/4$ results in images with S_0, S_2, and S_3, respectively. Modulation of LED, IG, and DG during integration time $t_{\text{int}} = t_1 - t_0$, which is set to 10 ms, contributes to the signal of a single row. After integration, sampling of "sampsig," pixel reset, and sampling of "samprst" are sequentially carried out. Alternating the 192 column addresses, CDS follows with appropriate toggling of "rstsf," "clamp," and "cb." Finally the resulting analog signals at "voutpos" and "voutneg" are digitized via an external ADC. This procedure repeats for the entire set of 108 rows. Full electronic rolling shutter timing is used to adjust for lighting, and the frame rate of the sensor reaches a maximum of 30 frames/s.

Functionality and performance of the test chip is characterized using a probe tester (IP750, Teradyne) and a custom built camera. Both a halogen lamp (Interaction) and

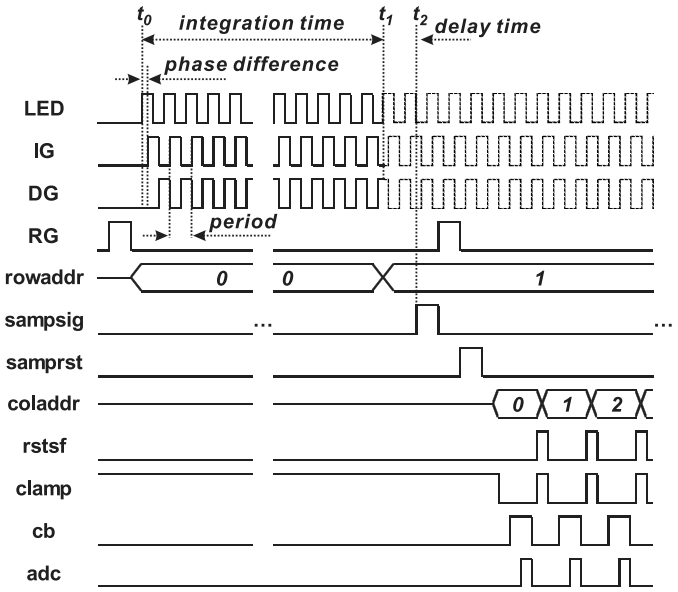

Fig. 7. Schematic timing diagram of concentric-gate pixel operation, starting from the first row with address 0. The LED, IG, and DG are modulating with periodicity p; the IG and DG are modulating out-of-phase from each other. The phase difference between LED and IG determines a phase-sensitive image, for example, $p/4$ phase difference results in an S_1 image. The integration time for each row is determined by the duration of LED lighting $t_1 - t_0$, indicated as a solid line for row address 0; the LED lighting and IG/DG modulation is indicated as a dotted line, and contributes to the signal in the second row with address 1. The delay time is defined as $t_2 - t_1$, which is normally set to 0 s. Pulse width and height are not to scale.

an array of LEDs (SFH4252, Osram) with a peak wavelength of 850 nm and a spectral bandwidth of 35 nm were used as light sources. The characteristics of the LED are analyzed by monitoring the amplitude modulation at various frequencies—controlled by a function generator (AFG3000C, Tektronix)—via the use of a photodetector with a rapid response time (Gigahertz-Optik, $X1_1$ Optometer, with an radiance detector RW-3705-4) and an oscilloscope. The modulation depth, defined as $m = (I_{\max} - I_{\min})/(I_{\max} + I_{\min})$ for maximum and minimum optical intensities $I_{\max}$ and $I_{\min}$, is approximately 100% below 1 MHz, but degrades to approximately 80% at 20 MHz. In addition, the rising and falling time required to reach 90% of $I_{\max}$ is approximately 10 ns.

Performance parameters including DE are characterized using images obtained from the custom-built camera and the characterization system, which consists of a field programmable gate array (FPGA), an image capture board (Simmian, Samsung Electronics), an LED array, and the appropriate lens and optics. A home-built rail-guide is used to vary the distance between the camera and the object. Image signal processing algorithms, including denoise, undistortion, removal of flying pixels, masking of pixels with excessive uncertainty, conversion to Cartesian distance, control of autoexposure and light source power, and automatic flicker avoidance are implemented at the system level, but beyond the scope of this paper.

IV. Results and Discussion

Statistical analysis of the signal level is performed to determine the 2-D performance of the test chip, as shown

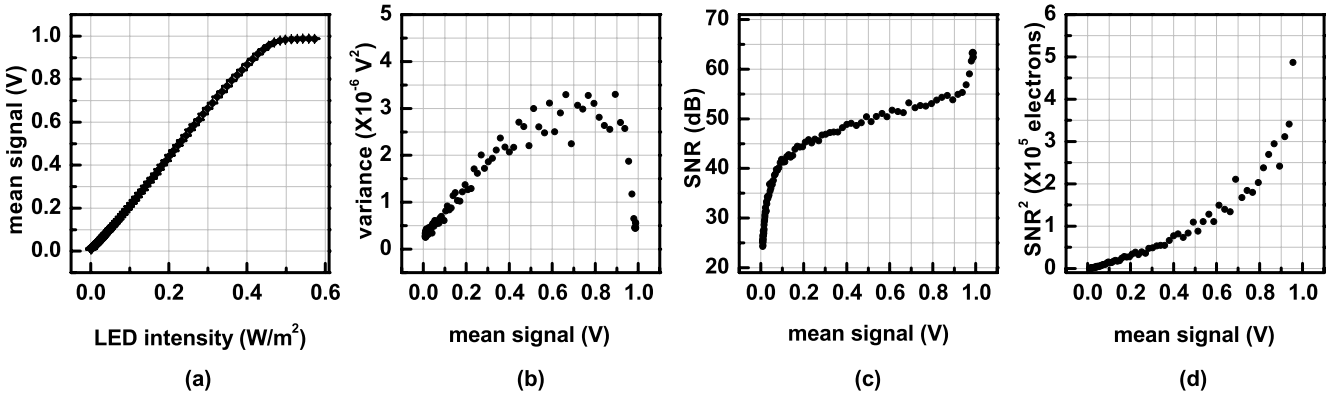

Fig. 8. Statistical analysis of signal level from test chip—photodetecting layers p^- and n^- are moderately doped using condition 4 as detailed in Table I—under a 20 MHz modulation of LED, IG, and DG. Bias levels applied to the IG and DG are 1.6 and 1.0 V, respectively. (a) 200 independent measurements are taken at each light intensity to obtain mean and standard deviation of signal level. (b) PTC is constructed to show the relationship between the variance and mean value of signals. (c) Equations (8) and (9) are used to obtain the dependence of signal-to-noise ratio. (d) Full-well-capacity on the mean of signal level.

in Fig. 8. An NIR LED modulating at 20 MHz is used to consider realistic operational conditions of the device. The maximum signal level is approximately 1 V, as shown in Fig. 8(a). For each signal level, the mean (m_{sig}), standard deviation (σ), and variance (σ^2) are obtained from 200 independent measurements. In addition, the photo-transfer curve (PTC), the relation between σ^2 and m_{sig}, is obtained as shown in Fig. 8(b); a clear linear relationship between σ^2 and m_{sig} exists for $m_{\text{sig}} < 0.5$ V, indicating that photon-shot noise is dominant in this signal range. Finally, the pixel conversion gain can be derived from the PTC slope, and is characterized as 7.2 μV/e$-$. The following equations are used for the investigation of SNR and SNR^2:

$$\text{SNR} = 20 \cdot \log\left(\frac{m_{\text{sig}}}{\sigma}\right) \tag{8}$$

$$\text{SNR}^2 = \left(\frac{m_{\text{sig}}}{\sigma}\right)^2. \tag{9}$$

Figure 8(c) shows the relationship between SNR and m_{sig}, and the maximum linear SNR measured is 50.4 dB. Furthermore, SNR^2 is dependent on m_{sig} as shown in Fig. 8(d), from which the linear full well capacity is determined to be 109500e$-$. From these parameters, our test chip shows a reasonable level of 2-D imaging performance.

On the other hand, to achieve an acceptable level of 3-D imaging performance, it is needed to assess parameters representing the demodulation process at the pixel level, such as A, B, DC, and the suppositional distance error DE$_s$; DE$_s$ is obtained from B and DC using (4), assuming $N = 0$. Figure 9 indicates that A, B, DC, and DE$_s$ are strongly dependent on both the modulation frequency and the doping conditions. When neither p^- nor n^- layer is embedded (condition 1), demodulation is not achievable. Once an additional p^- layer is introduced, demodulation becomes possible, as shown in the results for condition 2. To further increase the DC, especially at high frequencies, the charge transfer efficiency to both FD and DD should be improved, and is likely to result in an increased A, for the same level of B. Using a low n^- doped layer as in condition 3, we observe an improvement of A but a nearly threefold increase of B than that of condition 2. As a

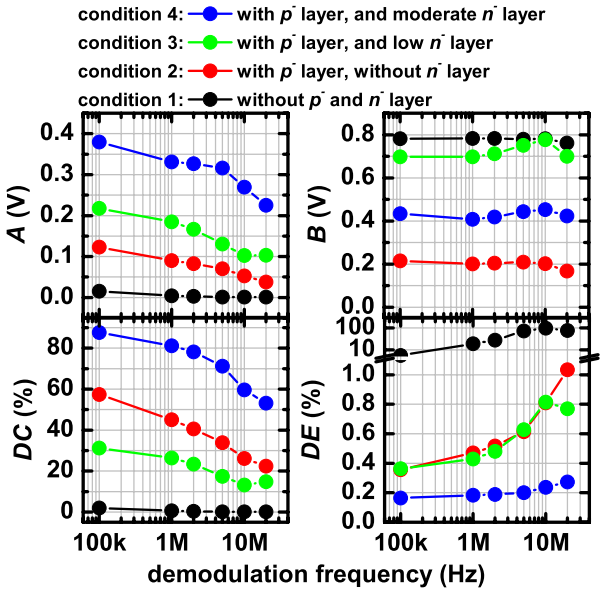

Fig. 9. Frequency dependence of A, B, DC, and suppositional DE, which follow the definitions from (4) to (5). Boron (B) and Arsenic (As) are used as dopants in the formation of photo-detecting layers as shown in Fig. 2, with incidence kinetic energies of 9 and 250 keV, respectively. Using condition 1—no p^- and n^- layer formation—as a reference, three different doping conditions for p^- and n^- layers are tested.

result, the DC of condition 3 is lower than that of condition 2, and the DE$_s$ for both conditions are comparable with each other over the entire frequency range observed. Because the charge transfer to FD and DD can be hindered by a potential barrier around FD and DD, we aim to resolve by tuning the n^- layer doping conditions. Using a moderately doped n^- layer (condition 4), we observe approximately 0.4 V for B, which is less than the 0.7 V observed in condition 3. On the other hand, A is approximately 0.4 V at 100 kHz, and drops to 0.2 V at 20 MHz. Consequently, the DC in condition 4 increases to as high as 90% and 53% at 100 kHz and 20 MHz, respectively, and exhibits a much improved DE$_s$ compared with that in conditions 2 and 3. Consequently,

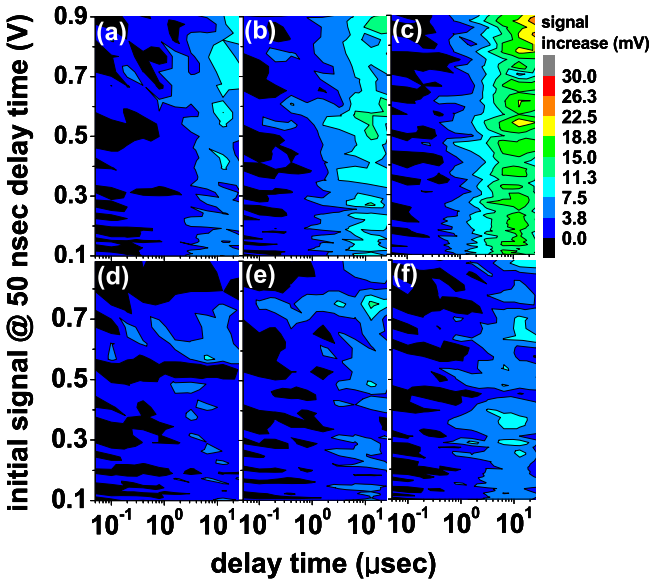

Fig. 10. Amount of signal increase as a function of delay time is measured at various demodulation frequencies of (a) and (d) 1 MHz, (b) and (e) 5 MHz, and (c) and (f) 20 MHz, using either an optimal doping condition (condition 4, lower panels) or a less-optimized condition (condition 3, upper panels).

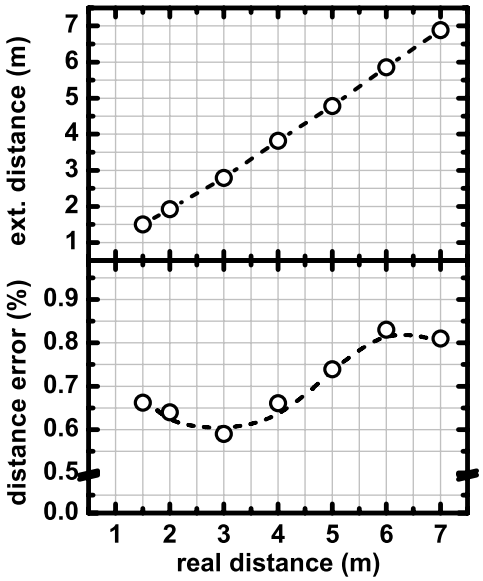

Fig. 11. (Top) extracted distance and (bottom) DE is evaluated for a camera-to-white paper distance of 1–7 m. The dotted lines are obtained via a Monte Carlo simulation, whose details are beyond the scope of this paper.

we successfully demonstrate a buried-channel structure for rapid charge transfer to FD and DD.

Of particular interest, the 53% DC value of our test chip with 28 μm pixel is higher than that of two-tap devices in previous reports; considering previous reports of 20% (in [2], measured at 10 MHz, pixel size of 65 $\times$ 21 μm^2), 26% (in [4], measured at 20 MHz, pixel pitch around 50 μm), and 38% (in [11], measured with 20 MHz modulating 780 nm LD, pixel pitch of 10 μm), the value obtained using our chip appears to be competitive. Although nearly 95% has been reported (in [8], measured with 860 nm LD, pixel size not known), the DC value is not comparable owing to a different pixel working principle.

It is reasonable to postulate that such high-frequency performance is facilitated by rapid charge transfer from IG to FD, as well as from DG to DD, as anticipated in Section II. This postulation can be confirmed by measuring the remnant signal electrons after integration, or signal lag. To characterize signal lag, S_0 is measured for a fixed LED intensity as a function of delay time, $t_{\text{delay}} = t_2 - t_1$; modulation of LED, IG, and DG are performed for a single row as indicated by the solid line in Fig. 7, and S_0 is sampled from the specific row. For the reference signal $S_{0,\text{ref}}$ measured at $t_{\text{delay}} = 50$ ns, it is possible to characterize a signal increase $\Delta S_{\text{lag}} = (S_0 - S_{0,\text{ref}})_{\text{single row}}$, indicative of signal lag caused by remnant photoelectrons under IG. Figure 10 shows ΔS_{lag} measured for various signal levels as a function of t_{delay}. In the case of nonoptimal doping, corresponding to the condition 3 in Fig. 9, a noticeable amount of the generated photoelectrons fails to arrive at FD during the illumination, especially at high frequency modulation. As seen in Fig. 10(a), under a demodulation frequency of 1 MHz, ΔS_{lag} is greater than 7.5 mV for t_{delay} greater than 10 μs and $S_{0,\text{ref}}$ greater than 0.4 V. When the modulation frequency increases, ΔS_{lag} increases significantly as shown in Fig. 10(b) and (c); for $t_{\text{delay}} = 10$ μs, 5 and 20 MHz modulations result in ΔS_{lag} in the range 7.5–11.3 and 15.0–18.8 mV, respectively, for the entire $S_{0,\text{ref}}$ signal level observed. This performance corresponds to a reduced level of A in condition 3 compared with that of condition 4, and explains why a pixel with nonoptimal doping layers exhibits a relatively reduced level of DC in Fig. 9. On the other hand, essentially no signal increase is observed for the pixel with a more optimized doping profile, corresponding to the condition 4 in Fig. 9, as shown in the lower panels in Fig. 10. Even at 20 MHz modulation, ΔS_{lag} is less than 7.5 mV, and only a limited number of $S_{0,\text{ref}}$ values exhibit 11.3 mV. This accounts for an enhanced DC in the observed modulation frequency range using an optimized doping layer, as shown in Fig. 10. We confirm the importance of optimal doping structure in the photodetecting layer and therefore use chips with the same underlying p- and n-layers of the optimized doping condition (condition 4) for all subsequent results following Fig. 10.

Figure 11 shows the dependency of extracted distance and—obtained using (1) to (3)—on real geometric distance; the distance between the camera and object is varied from 1 to 7 m. At each distance, 100 independently captured images were statistically analyzed to characterize the DE value. We report that the precision of the extracted distance is higher than 99%, whereas DE is less than 0.9% over the distance analyzed. This performance is achieved by significantly high values of DC, as well as by reasonable 2-D performance of the concentric gate pixel array.

Furthermore, DE exhibits no monotonic increase or decrease as a function of geometric distance. For distances below 3 m, an increase in DE is observed as the distance is decreased owing to pixel saturation; when the integration time or camera lens aperture is reduced, DE is reduced. For distances above 3 m, an increase in DE is observed as the distance is decreased

Fig. 12. 3-D image is obtained from one of the authors, whose body is located at a distance of 3 m from the camera. The overlaid solid black line is derived using an edge-detection algorithm during image signal processing. The image is taken using an objective lens of F#1.2 with frame rate of 30 frames/s and an IR band-pass filter that allows for a near-complete transmission of photon between 820 and 880 nm.

TABLE II
SUMMARY TABLE FOR PERFORMANCE

parameters	values
chip size	7.8 mm × 5.0 mm
pixel array	192(columns) × 108 (rows)
pixel size	28 μm × 28 μm
V_{dd}	2.8 V
pixel conversion gain	7.2 μV/e-
signal to noise ratio	50.4 dB
linear full well cap	109500 e-
dark current at 35°C, 20MHz	68.4 e-/msec
DC at 20MHz	$>$ 50%
DE at 7 m	0.8%

due to a reduced light intensity, and consequent offset B. While we realize that SNR and other statistical terms such as PRNU may play an important role, statistical simulation indicates that the reduced light intensity at further distances is a far more predominant cause for an increase in DE.

An image is obtained using the sensor and subsequent signal processing yields a 3-D image as shown in Fig. 12. Flicker noise due to ambient illumination from incandescent lamps and artifacts created by background illumination are effectively removed during signal processing. It should be noted that object features in addition to detailed distance information are clearly visible within the 1–7 m distance range. In essence, the CG pixel-based sensor performs at a satisfactory level, leading the way for further expansion as a motion detection interface for gesture recognition applications.

V. CONCLUSION

A ToF-3-D image sensor using novel concentric photogate pixels with single-tap operation is described. Through the use of CG, we demonstrate a substantially improved DC, reaching levels as high as 53% at 20 MHz with a 28 μm pixel pitch. The sensor performance of the CG pixel array is summarized in Table II. Coupled with other sensor specifications, the CG pixel may play a central role in several fields such as motion detection and gesture control applications.

Although the concentric gate pixel does not currently allow for suppression of kTC noise—a feature currently equipped in modern CIS devices [14]—the addition of more concentric rings for signal integration and transfer to FD would allow for operation in lower light illuminance. However, the complexity and likely reduction in DC does not appear to merit this approach, and external CDS using memory could prove to be more effective and may be investigated in the future.

Also, though the CG pixel shows acceptable demodulation performance, it is important to understand the physical origins behind the observed sensor characteristics, such as those detailed in Figs. 8 to 10. For instance, the significant decrease of A and DC as a function of modulation frequency observed in Fig. 9 may be related to frequency-dependent switching behaviors of metal-oxide-silicon capacitive devices [15]. A detailed analysis is underway, and will be reported elsewhere.

In addition to improvements made to the pixel, an optimized system design can significantly improve the sensor performance. Use of a high-speed modulating light source is an example. Though not discussed explicitly in this paper, we observed that the modulation depth m of LED light degrades to less than 80% at 10 MHz, with a rising and falling time of approximately 10 ns. Such poor modulation characteristics may in part explain the degradation of A and DC with increasing frequency as shown in Fig. 9. From this perspective, the use of an LD as a modulating light source, which typically guarantees high-speed modulation even up to 100 MHz [8], [11], is highly desirable; performance characterization studies of the CG pixel at frequencies higher than 20 MHz and a significantly reduced DE may be achievable through this platform.

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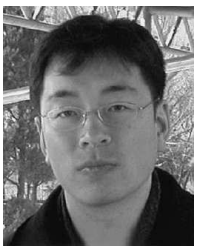

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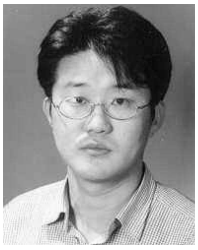

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